

## **METHODS OF FABRICATING A SEMICONDUCTOR**

### **DEVICE HAVING A METAL GATE PATTERN**

#### **CROSS REFERENCE TO RELATED APPLICATIONS**

**[0001]** This U.S. non-provisional application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 2002-57456, filed on September 19, 2002, in the Korean Intellectual Property Office, the contents of which are incorporated herein by reference in their entirety.

#### **BACKGROUND OF THE INVENTION**

##### Field of the Invention

**[0002]** The present invention relates generally to methods of fabricating semiconductor devices having metal gate patterns, and more particularly to a method of fabricating a semiconductor that includes selective oxidation to reduce damage to the metal gate pattern caused by dry etching.

##### Description of the Related Art

**[0003]** Due to a continuing interest in increasing the integration density of semiconductor devices, the dimensions of various structural elements such as capacitors and

gate electrodes utilized to form such semiconductor devices also tend to be reduced.

Because of the increase in the integration density, materials having a low resistivity have been used to decrease signal delay. For example, metal gates which use a metallic material having a low resistivity have been utilized for lowering the sheet resistance of a gate and lowering the height of a gate stack. These studies have led to the development of metal gates incorporating a tungsten/tungsten nitride/polysilicon stack structure.

**[0004]** Forming a metal gate stack may include forming a gate insulating layer on a silicon substrate, sequentially stacking a polysilicon layer, a tungsten nitride layer, a tungsten layer, and a gate mask layer, forming an etch mask using a photolithographic process, and performing a dry etching process. However, the surface of the silicon substrate and the sidewalls of the metal gate pattern exposed to the dry etching process may be damaged by the dry etching process. An oxidation process (e.g., a "gate polysilicon reoxidation process") may be performed to correct damage caused by the dry etching process. One example of a conventional gate polysilicon reoxidation process is a rapid thermal process performed in an atmosphere of a gas mixture of O<sub>2</sub> gas and NF<sub>3</sub> gas, such as is described in U.S. Patent No. 5,672,525, the contents of which are incorporated by reference in their entirety.

**[0005]** The gate polysilicon reoxidation process may be carried out using a dry oxidation process. In a dry oxidation process, however, the exposed surface of a tungsten layer, which may be a metal layer included in the metal gate pattern, may be oxidized by the dry oxidation process. This oxidation of the tungsten layer may result in a reduction in the effective sectional area of the gate. As a result, the resistance of a gate line (e.g., a conductive line), may be increased, which may cause a delay of a signal transmission.

Further, the oxidation of the tungsten layer may cause the metal gate pattern to have a poor vertical profile.

**[0006]** FIG. 1 is a graph illustrating the thickness of a gate oxide layer with respect to the gate length after a conventional selective oxidation was performed. Referring to FIG. 1, selective oxidation was performed on a gate pattern that included a gate oxide layer and a polysilicon layer formed on a silicon substrate. The selective oxidation was performed in a rapid thermal process (RTP) apparatus and a furnace apparatus under various process conditions. As shown in FIG. 1, when the gate length was 180 nm or more, the gate oxide layer had a thickness of about 55 Å at approximately the center of the gate pattern. When the gate length was 90 nm or less, the gate oxide layer had a thickness of from about 85 to about 150 Å. As reflected in these results, when the gate length is small, the selective oxidation process may result in a dramatic and undesirable increase in the thickness of the gate oxide layer due to a “bird’s beak” effect.

[0007] Selective oxidation using a partial pressure ratio of  $\text{H}_2\text{O}$  and  $\text{H}_2$  in an  $\text{H}_2$ -rich wet oxidation process may oxidize a polysilicon layer and a silicon substrate and may reduce the oxidation of the metal layers included in the metal gate pattern. As reflected in Table 1, below, both the oxidation rates for silicon and polysilicon and the ratios of those rates can vary depending on the particular oxidation process employed. Table 1 provides the results obtained by measuring the thicknesses of oxide layers formed on the surfaces of a silicon substrate and a polysilicon layer, after performing both a conventional dry oxidation and selective oxidation processes, respectively.

Table 1

Classification	Dry oxidation	Selective oxidation	
	850 °C., 50Å	850 °C., 50Å	850 °C., 30Å
Thickness T1 of oxide layer on silicon substrate	63.14Å	50.53Å	30.86Å
Thickness T2 of oxide layer on polysilicon layer	144.84Å	158.59Å	93.16Å
T2/T1	2.29	3.14	3.02

[0008] As shown Table 1, the silicon substrate and the polysilicon layer had an original thickness of 50 Å. Each of the silicon substrate and the polysilicon layer were oxidized by dry oxidation and selective oxidation at 850 °C. When the dry oxidation was performed, the oxide layer formed on the polysilicon layer was approximately 2.2 times as thick as the oxide layer formed on the silicon substrate. By comparison, when selective

oxidation was performed, the oxide formed on the polysilicon layer was approximately 3.1 times as thick as the oxide layer formed on the silicon substrate.

**[0009]** When the silicon substrate and the polysilicon layer had an original thickness of 30 Å and selective oxidation was performed, the oxide layer formed on the polysilicon layer was approximately 3.0 times as thick as that formed on the silicon substrate after wet selective oxidation (e.g., the oxidation rate (T2/T1) of the polysilicon layer was approximately 3.0 times as high as that of the silicon substrate.

**[0010]** FIG. 2A is a photograph illustrating the thickness of a gate oxide layer at the edge of a gate pattern (with no capping layer) according to a conventional selective oxidation process. FIG. 2B is a photograph illustrating the thickness of the gate oxide layer at the center of the gate pattern shown in FIG. 2A. Prior to conducting the selective oxidation process, the gate oxide layer had a thickness of approximately 55 Å. As shown in FIG. 2A, after the selective oxidation process, the gate oxide layer had a thickness of approximately 98 Å at the edge of the gate pattern and a thickness of approximately 90 Å at the center of the gate pattern. Thus, the thickness of the gate oxide layer, both at the edge of the gate pattern and at the center of the gate pattern, was increased. As a result, the gate oxide layer will have an increased likelihood of exhibiting punch-through failures.

**[0011]** Although conventional selective oxidation may correct damage caused by etching when a metal gate is used, dry selective oxidation fails to control the thickness of the gate oxide layer, and poses a particular problem for designs utilizing smaller gate lengths. Also, since the increased gate oxide layer is typically an oxidized polysilicon layer, the quality of the gate oxide layer may be degraded.

### **SUMMARY OF THE INVENTION**

**[0012]** An exemplary embodiment of the present invention provides a method of fabricating a semiconductor device having a metal gate pattern. A metal gate material layer may be deposited on a substrate, e.g., a silicon substrate, with a metal gate pattern then being formed using a dry etching process. The dry etching used to form the metal gate layer may damage the exposed surface of the silicon layer and the edges of the metal gate layer. The metal gate pattern may be formed of layers, e.g., sequential layers, of a gate insulating layer (e.g., a gate oxide layer), a first conductive layer (e.g., a polysilicon layer), a second conductive layer (e.g., a tungsten nitride layer), a third conductive layer (a tungsten layer), and a gate mask layer (e.g., an insulating silicon nitride layer).

**[0013]** The gate insulating layer may be formed of one or more insulating materials including  $\text{SiO}_2$ ,  $\text{SiON}$ ,  $\text{SiN}$ ,  $\text{HfO}_x$ ,  $\text{ZrO}_x$  and  $\text{HfAlO}_x$ , metal oxide, metal silicate, and other high k-dielectric materials. The second conductive layer and the third conductive layer may be formed of a metal layer that includes at least one material that has a low resistance. Suitable examples of such low resistance materials include W, Ni, Co, TaN, Ru-Ta, TiN, Ni-Ti, Ti-Al-N, Zr, Hf, Ti, Ta, Mo, MoN, WN, Ta-Pt and Ta-Ti.

**[0014]** A first capping layer may then be formed on the surface of the substrate and the metal gate pattern. The first capping layer may be formed to a thickness of approximately 500 Å or less and a second capping layer may be deposited on the first capping layer. Suitable examples of the first and second capping layers include  $\text{SiO}_x$ ,  $\text{SiN}_x$

and Si<sub>3</sub>N<sub>4</sub>. When a silicon oxide layer is deposited as the first capping layer, the oxidation of the metal layers in the metal gate oxide layer may be reduced.

**[0015]** Spacers may be formed on sidewalls of the metal gate pattern after the formation of the capping layer(s). After the formation of the first capping layer, the first capping layer may be etched, e.g., anisotropically etched, to form first capping spacers on the sidewalls of the metal gate pattern. If a second capping layer is present on the first capping layer, the second capping layer may be etched initially, e.g., anisotropically etched, to form second capping spacers.

**[0016]** Selective oxidation may be performed to reduce the damage to the exposed surface of the silicon substrate and edges of the metal gate pattern caused by the dry etching process conducted when forming the metal gate pattern. The selective oxidation may be a wet oxidation process using a partial pressure of H<sub>2</sub>O and H<sub>2</sub>. In addition, the selective oxidation may be performed in an H<sub>2</sub>-rich atmosphere. The selective oxidation may reduce the oxidation of the second conductive layer (e.g., tungsten nitride layer) and the third conductive layer (e.g., tungsten layer) in the metal gate pattern and may selectively oxidize the surface of the silicon substrate and the first conductive layer (e.g., a polysilicon layer). In addition, the capping layer may reduce the diffusion of oxidants during selective oxidation. As a result, damage to the edges of the gate pattern may be reduced and the occurrence of punch-through of the gate insulating layer may be lowered.

**[0017]** In accordance with an aspect of the present invention, there is provided a method of fabricating a semiconductor device with a metal gate pattern, comprising forming a gate insulating layer on a silicon substrate and then depositing a metal gate material layer

including at least a metal layer on a silicon substrate where the gate insulating layer is formed.

Next, the metal gate material layer is etched so as to form a metal gate pattern. A capping layer is then formed on the metal gate pattern. Selective oxidation is carried out to cure damages caused by the etching process for forming the metal gate pattern. Thus, the oxidation of the metal layer included in the metal gate pattern is prevented and a material containing silicon is selectively oxidized.

**[0018]** Forming the silicon oxide layer on the entire surface of the semiconductor substrate where the metal gate pattern is formed, such that the metal layer included in the metal gate pattern is not oxidized, may comprise loading the silicon substrate where the metal gate pattern is formed into a reaction chamber in which a deposition process can be carried out. Next, a gas containing  $N_2$  capable of decomposing at a low temperature is injected into the reaction chamber to create an  $N_2$  atmosphere. A silicon source gas and an oxygen gas are injected into the reaction chamber so as to deposit the silicon oxide layer on the metal gate pattern.

**[0019]** The gas used to form the nitrogen atmosphere gas will typically not contain any oxygen and is preferably ammonia ( $NH_3$ ). The silicon source gas may be one or more silicon-containing gases such as  $SiH_4$ ,  $Si_2H_6$ , DCS (Dichlorosilane), TCS (Trichlorosilane) or HCD (Hexachlorodisilane). The oxygen source gas may include one or more gases including nitrogen, such as  $N_2O$  or  $NO$ , and/or gases that do not contain nitrogen, such as  $O_2$ .

**[0020]** Meanwhile, the silicon source gas may be injected before or at the same time as the oxygen source gas. The injection of the nitrogen atmosphere gas may be stopped after or at the same time as the injection of the oxygen source gas. Alternatively, the



injection of the nitrogen atmosphere gas may be stopped before the injection of the silicon source gas or the oxygen source gas.

**[0021]** Meanwhile, the silicon oxide layer may be deposited under a low pressure of 0.01 to 500 Torr. To set the process pressure within the range of 0.01 to 500 Torr, a pumping rate of an exhausting pump and flow rates of process gases, such as the silicon source gas and the oxygen source gas, can be properly adjusted.

**[0022]** Also, the silicon oxide layer may be deposited at a high temperature of 500 °C. or higher using thermal chemical vapor deposition (thermal CVD). As long as flow rates of process gases are greatly reduced to slow down a deposition rate, the silicon oxide layer may be deposited by plasma enhanced CVD (PECVD) using a remote plasma.

**[0023]** Forming the capping layer may further comprise forming silicon oxide spacers on sidewalls of the metal gate pattern by anisotropically etching the silicon oxide layer after depositing the silicon oxide layer. Forming the capping layer may further comprise depositing a silicon nitride layer on the entire surface of the silicon oxide layer after depositing the silicon oxide layer. Forming the capping layer may further comprise forming silicon nitride spacers on the silicon oxide layer formed on the sidewalls of the metal gate pattern by anisotropically etching the silicon nitride layer after depositing the silicon nitride layer. Also, forming the capping layer may comprise forming a silicon nitride layer on the entire surface of the semiconductor substrate where the metal gate pattern is formed such that the metal layer included in the metal gate pattern is not oxidized.

**[0024]** According to the present invention, a capping layer is further deposited on a metal gate pattern, before applying selective oxidation, which is a reoxidation process

required for a semiconductor device with the metal gate pattern including a metal layer.

Thus, the capping layer can suppress diffusion of oxidants during the selective oxidation.

As a result, while damages caused on edges of the gate pattern during the etching process for forming the metal gate pattern can be cured, a punch-through of the gate insulating layer can be prevented.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0025]** Exemplary embodiments of the present invention will be readily understood with reference to the following detailed description thereof provided in conjunction with the attached drawings in which:

**[0026]** FIG. 1 is a graph illustrating the thickness of a gate oxide layer with respect to the gate length after a conventional selective oxidation process;

**[0027]** FIG. 2A is a photograph illustrating the thickness of a gate oxide layer at the edge of a gate pattern after a conventional selective oxidation process had been performed;

**[0028]** FIG. 2B is a photograph illustrating the thickness of the center of the gate oxide layer shown in FIG. 2A;

**[0029]** FIG. 3 is a flowchart illustrating a method of fabricating a semiconductor device having a metal gate pattern according to at least one exemplary embodiment of the present invention;

**[0030]** FIG. 4 is a flowchart illustrating a method of fabricating a semiconductor device having a metal gate pattern according to at least one other exemplary embodiment of the present invention;

**[0031]** FIG. 5 is a cross-sectional view illustrating an example of a metal gate pattern according to an exemplary embodiment of the present invention;

**[0032]** FIG. 6 is a cross-sectional view illustrating a first capping layer on the metal gate pattern illustrated in FIG. 5 according to at least one exemplary embodiment of the present invention;

**[0033]** FIG. 7 is a cross-sectional view illustrating first capping spacers formed on the metal gate pattern illustrated in FIG. 5 according to at least one exemplary embodiment of the present invention;

**[0034]** FIG. 8 is a cross-sectional view illustrating a first and a second capping layer formed on the metal gate pattern illustrated in FIG. 5 according to at least one exemplary embodiment of the present invention;

**[0035]** FIG. 9 is a cross-sectional view illustrating second capping spacers formed on a first capping layer according to at least one exemplary embodiment of the present invention;

**[0036]** FIG. 10 is a photograph illustrating a cross-section of a cell region of a semiconductor device according to at least one exemplary embodiment of the present invention;

**[0037]** FIG. 11 is a photograph illustrating a cross-section of a peripheral region of a semiconductor device according to at least one exemplary embodiment of the present invention;

**[0038]** FIG. 12A is a photograph illustrating the thickness of a gate oxide layer at the edges of a gate pattern according to at least one exemplary embodiment of the present invention; and

**[0039]** FIG. 12B is a photograph illustrating the thickness of the center of the gate oxide layer shown in FIG. 12A.

#### **DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS**

**[0040]** Exemplary embodiments of the present invention will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough and complete and fully conveys the concept of the invention to those skilled in the art. In the drawings, the shape of the elements may be exaggerated for clarity, and the same reference numerals in different drawings represent the same elements.

**[0041]** Further, it will be understood that when a layer is referred to as being “on” another layer or substrate, it can be located directly on the other layer or substrate, or intervening layers may also be present. It will also be understood that when a layer is

referred to as being “directly on” another layer or substrate, intervening layers are not present. It is to be further understood that when two steps are referred to as occurring at substantially the same time, the two steps may occur at the same time or at substantially the same time.

**[0042]** FIG. 3 is a flowchart illustrating a method of fabricating a semiconductor device having a metal gate pattern according to at least one exemplary embodiment of the present invention. FIGS. 5 and 6 are cross-sectional views illustrating a method of fabricating a semiconductor device according to at least one exemplary embodiment of the present invention.

**[0043]** Referring to FIG. 3, in step S10, a metal gate material layer which includes at least one metal layer having a low resistance may be first deposited on a substrate. The substrate may be any suitable substrate, such as a silicon substrate formed of single crystal silicon. In step S20, a metal gate pattern may then be formed from the metal gate material layer by a conventional etching process, e.g., a dry etching process using in combination with a photolithographic process. When the metal gate pattern is formed using a dry etching process, damage will typically be sustained on the exposed surface of the silicon substrate and at the edges of the metal gate pattern.

**[0044]** Various metal gate patterns which include at least one metal layer can be used in the exemplary methods of the present invention. Suitable examples of the metal gate pattern include a stack of a gate mask/tungsten/tungsten nitride/polysilicon/gate oxide layer, a metal/barrier metal/polysilicon/gate insulating layer, a metal/polysilicon/gate insulating layer, a metal/barrier metal/gate insulating layer, and a metal/gate insulating layer. Each of these metal gate patterns may also include an insulating gate mask layer formed of silicon nitride.

**[0045]** In addition, the metal gate pattern may be a polysilicon layer formed on a gate insulating layer. If the metal gate pattern is formed on a silicon substrate, the surface of the silicon substrate may be oxidized during a reoxidation process, which may correct the damage at edges of the gate pattern. Accordingly, the present invention may also be applied to a metal gate pattern obtained by forming a metal layer directly on a gate insulating layer.

**[0046]** An example of a metal gate pattern according to at least one exemplary embodiment of the present invention is illustrated in FIG. 5. In this exemplary embodiment, the metal gate pattern is formed of layers, e.g., sequential layers, of a gate insulating layer 12 (e.g., a gate oxide layer), a first conductive layer 14 (e.g., a polysilicon layer), a second conductive layer 16 (e.g., a tungsten nitride layer), a third conductive layer 18 (a tungsten layer), and a gate mask layer 20 (e.g., an insulating silicon nitride layer) on a substrate 10. The gate insulating layer 12 may be formed from  $\text{SiO}_2$ , SiON, SiN,  $\text{HfO}_x$ ,  $\text{ZrO}_x$ , and  $\text{HfAlO}_x$ , metal oxide, metal silicate, or other suitable high k-dielectric materials. The second conductive layer 16 and the third conductive layer 18 may be formed from a metal layer that includes at least one material that has low resistivity. Suitable examples of such low resistivity materials include, but are not limited to, W, Ni, Co, TaN, Ru-Ta, TiN, Ni-Ti, Ti-Al-N, Zr, Hf, Ti, Ta, Mo, MoN, WN, Ta-Pt, and Ta-Ti. In addition, the materials and the thickness of the layers and the processes may be varied depending on the deposition conditions, such as the type of the reaction chamber, the pressure, temperature, energy, duration, flowrates and the specific process gases used and the sequence in which they are introduced to the reaction chamber. Further, the thickness of the metal layer may vary according to the metal and materials used.

**[0047]** In step S30, a first capping layer 22 may then be deposited on the surface of the silicon substrate 10 and the metal gate pattern 30 (see FIG. 6). The first capping layer 22 will typically be formed to a thickness of about 500 Å or less. In at least one exemplary embodiment of the present invention, the first capping layer has a thickness of approximately 100 Å. A second capping layer 24 of similar thickness may be deposited on the first capping layer 22 (see FIG. 8). Suitable examples of the first and second capping layers 22, 24 include, but are not limited to, SiO<sub>x</sub>, SiN<sub>x</sub> and SiON. In at least one exemplary embodiment of the invention, the first capping layer 22 is formed of a silicon oxide layer and the second capping layer 24 is formed of a silicon nitride layer.

**[0048]** When a silicon oxide layer is deposited as the first capping layer 22 on the metal gate pattern 30, the oxidation of the metal layers included in the metal gate pattern (e.g., a tungsten or a tungsten nitride layer) may be reduced. Thus, the capping layer 22 may be capable of lowering the amount of oxidants diffused during an oxidation process performed on a metal gate pattern without oxidizing the metal layers included in the metal gate pattern. As a result, damage to the edges of the metal gate pattern caused by the oxidation process may be reduced. In addition, the oxidation of a gate insulating layer of the metal gate pattern may be reduced which may lower the occurrence of punch-through in the gate insulating layer. Consequently, more reliable semiconductor devices may be fabricated through the use of one or more capping layers.

**[0049]** Further, according to exemplary embodiments of the present invention, the surface of a metal layer, which may be exposed to a deposition atmosphere during the formation of a capping layer, is not oxidized. Thus, both the resistance of the metal layer

and the vertical profile of the gate line may be maintained during subsequent oxidation processes.

**[0050]** In step S40, selective oxidation may be performed to correct damage to the exposed surface of the silicon substrate 10 and edges of the metal gate pattern 30 caused by the dry etching process conducted when forming the metal gate pattern 30. The selective oxidation may be a wet oxidation process using a partial pressure of  $H_2O$  and  $H_2$  or may be performed in an  $H_2$ -rich atmosphere. The selective oxidation may reduce the oxidation of the second conductive layer 16 (e.g., tungsten nitride layer) and the third conductive layer 18 (e.g., tungsten layer) in the metal gate pattern and may selectively oxidize the surface of the silicon substrate 10 and the first conductive layer 14 (e.g., a polysilicon layer).

**[0051]** Subsequent processes for fabricating semiconductor devices may then be performed. For example, impurity ions may be implanted into the substrate 10 by using the metal gate pattern 30 as an ion implantation mask, thereby forming an impurity region, e.g., a lightly doped region.

**[0052]** FIG. 4 is a flowchart illustrating a method of fabricating a semiconductor device having a metal gate pattern according to at least one exemplary embodiment of the present invention. Steps S10 – S30 are conducted in the same manner as described above with reference to FIG. 3.

**[0053]** In step S35, spacers may be formed on the sidewalls of the metal gate pattern 30 after the formation of the capping layer(s). For example, after depositing the first capping layer 22, the capping layer 22 may be etched, e.g., anisotropically etched, to form first capping spacers 22a on the sidewalls of the metal gate pattern 30 (see FIG. 7). If a



second capping layer 24 is present on the first capping layer 22, the second capping layer 24 may be etched, e.g., anisotropically etched, to form second capping spacers 24a as illustrated in FIG. 9. Once the spacers, e.g., first capping spacers 22 and/or second capping spacers 24, are formed, in step S40, selective oxidation may be performed as described above to selectively oxidize the substrate 10 and the first conductive layer 14.

**[0054]** An exemplary embodiment of the present invention in which a silicon oxide layer (e.g., a capping layer) is formed on a metal gate pattern with a reduction in the amount of oxidation of the surfaces of the metal layers, e.g., the second conductive layer 16 (tungsten nitride layer) and the third conductive layer 18 (tungsten layer) will now be described in detail.

**[0055]** The substrate 10, including the metal gate pattern 30, may be loaded into a reaction chamber in which a deposition process, e.g., a chemical vapor deposition (CVD) process, may be performed. Suitable types of CVD processes include plasma enhanced CVD (PE-CVD), high density plasma CVD (HDP-CVD), thermal CVD, laser CVD, and hot filament CVD (HF-CVD). Exemplary embodiments of the present invention may be applied to processes with plasma by reducing the flow rates of the process gases or by reducing the deposition speed using a remote plasma source.

**[0056]** When a PE-CVD process is used, the silicon oxide layer may be formed at a temperature of from approximately 400 °C. to approximately 500 °C. At these temperatures, an oxygen gas used to form the silicon oxide layer may not decompose and the metal layers may not be oxidized. In addition, the silicon source gas may be supplied at substantially the same time as igniting the plasma to form the silicon oxide. Thus, the silicon may react with

the oxygen to deposit the silicon oxide layer with a reduction in the oxidation of the metal layers.

**[0057]** The silicon oxide layer may also be formed using a PE-CVD process at a temperature of approximately 750 °C. If the oxygen source gas and the silicon source gas are substantially injected at substantially the same time, the silicon oxide layer may be deposited with a reduction in the oxidation of the metal layers.

**[0058]** The silicon oxide layer may be formed using a low pressure CVD process at a temperature of approximately 750 °C. The silicon source gas may be supplied just before the oxygen source gas to deposit silicon oxide layer with a reduction in the oxidation of the metal layers.

**[0059]** The reaction chamber of the present embodiment is preferably one of a single-wafer-type chamber and a batch-type chamber. Experimental conditions may vary depending on the types of equipment used, and these experimental conditions would be easily determined and adjusted by one of skill in the art. Although a CVD process in a single wafer type reaction chamber is described herein, a furnace having a large capacity and the ability to control the pressure, temperature, and flow rates of gases entering into the furnace may alternatively be used.

**[0060]** Next, the reaction chamber may be maintained in a nitrogen atmosphere. In order to maintain a nitrogen atmosphere, a nitrogen source gas, e.g., a gas that includes at least nitrogen, may be supplied to the reaction chamber, e.g., at a constant flow rate, for a period of time. The nitrogen atmosphere gas may decompose at a low temperature and may be a compound that does not include oxygen. The absence of oxygen may reduce the

oxidation of the metal layer, and, as a result, the oxidation of metal layers present in the gate electrode (e.g., a tungsten layer) may be reduced or eliminated. In at least one exemplary embodiment of the present invention, an ammonia ( $\text{NH}_3$ ) gas may be used as the nitrogen source gas. Other suitable nitrogen source gases would be easily identified by those of skill in the art.

**[0061]** A silicon source gas and/or an oxygen source gas may then be supplied to the reaction chamber in the nitrogen atmosphere to form a silicon oxide layer (e.g., capping layer 22) on the metal gate pattern 30. Suitable silicon source gases include, but are not limited to,  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$ , DCS (dichlorosilane), TCS (trichlorosilane), and HCD (hexachlorodisilane). Suitable oxygen source gases include, but are not limited to,  $\text{N}_2\text{O}$ , NO, and  $\text{O}_2$ . In one exemplary embodiment of the present invention, a silane gas ( $\text{SiH}_4$ ) may be used as the silicon source gas and oxygen may be used as the oxygen source gas.

**[0062]** A silicon nitride layer (e.g., the second capping layer 24), may be formed on the silicon oxide layer (e.g., first capping layer 22) by performing a general CVD process. As described above, suitable types of CVD processes include plasma enhanced CVD (PE-CVD), high density plasma CVD (HDP-CVD), thermal CVD, laser CVD, and hot filament CVD (HF-CVD).

**[0063]** A process for establishing and maintaining a nitrogen atmosphere in the reaction chamber and forming the silicon oxide layer (e.g., capping layer 23) on the metal gate pattern 30 by supplying a silicon source gas and an oxygen source gas will now be described.

**[0064]** As discussed above, a nitrogen source gas, e.g., ammonia, may be supplied to the reaction chamber to establish a nitrogen atmosphere within the reaction chamber. The supply of the nitrogen source gas may be stopped after or at substantially the same time as the supply of the oxygen gas into the reaction chamber is initiated. Alternatively, the supply of the nitrogen source gas may be stopped before the oxygen source gas is supplied to the reaction chamber. The introduction of the silicon source gas into the reaction chamber may be initiated either before or at substantially the same time as the oxygen source gas is introduced. Other suitable sequences for the supply of the functional gases to the reaction chamber may be easily determined by one of skill in the art.

**[0065]** Experimental conditions and parameters in methods according to exemplary embodiments of the present invention may vary according to the type and the size of reaction chambers, and the types and the pressures of the process gases. For example, when the reaction chamber is a single-wafer-type chamber, the temperature may range from approximately 500 to approximately 850 °C., the pressure may range from approximately 100 to approximately 300 Torr, the flow rate of the nitrogen source gas may range from approximately 50 to approximately 500 sccm, the flow rate of the silicon source gas may range from approximately 1 to approximately 10 sccm, and the flow rate of the oxygen source gas may range from approximately 500 to approximately 5000 sccm. In another exemplary embodiment, the temperature may range from approximately 500 to approximately 850 °C., the pressure may range from approximately 0.1 to approximately 3 Torr, the flow rate of the nitrogen source gas may range from approximately 50 to approximately 1000 sccm, the flow rate of the silicon source gas may range from

approximately 1 to approximately 50 sccm, and the flow rate of the nitrogen source gas may range from approximately 50 to approximately 1000 sccm.

**[0066]** When the reaction chamber is a batch-type chamber, the temperature may range from approximately 500 to approximately 850 °C., the pressure may range from approximately 0.1 to approximately 2 Torr, the flow rate of the nitrogen source gas may range from approximately 50 to approximately 1000 sccm, the flow rate of the silicon source gas may range from approximately 5 to approximately 200 sccm, and the flow rate of the oxygen source gas may range from approximately 50 to approximately 1000 sccm.

**[0067]** If the supply of the nitrogen source gas is stopped before the oxygen source gas is supplied to the reaction chamber, the time period between the termination of the nitrogen source gas supply and the initial introduction of the oxygen source gas is preferably brief so that the nitrogen atmosphere in the reaction chamber is substantially maintained. This allows the silicon source gas and the oxygen source gas to be introduced into the reaction chamber under a nitrogen atmosphere.

**[0068]** FIGS. 10 and 11 are scanning electron microscope (SEM) photographs illustrating semiconductor devices fabricated according to exemplary embodiments of the present invention. FIG. 9 is a photograph of a cross-section of a cell region of semiconductor device in which metal gate patterns are positioned in close proximity to each other and the gate length is small. FIG. 10 is a photograph of a cross-section of a peripheral region of a semiconductor device in which metal gate patterns are not located close to each other and the gate length is large.

**[0069]** Referring to FIGS. 10 and 11, in both cases, selective oxidation was conducted after a silicon oxide layer was formed on a metal gate pattern according to exemplary embodiments of the present invention. A polysilicon layer may be formed to a certain thickness (e.g., a thick layer) on the surface (e.g., the entire surface) of the silicon substrate and the silicon substrate may be vertically sectioned. The sectioned silicon substrate may then be HF-processed. After HF-processing, the silicon oxide layer may be selectively etched at a faster rate than the polysilicon or other material layers of the metal gate pattern. After forming a silicon oxide layer as the capping layer to a thickness of about 100 Å, even if the selective oxidation is carried out, while the tungsten layer 18 and the tungsten nitride layer 16 are not oxidized, only the silicon substrate 10 and polysilicon layer 14 are oxidized. In FIGS. 10 and 11, dark lines along the gate line pattern depict the deposited silicon oxide layer and the oxidized silicon substrate and polysilicon layer. Thus, the silicon substrate and the polysilicon layer may be selectively oxidized with a reduction in the oxidation of the metal layers the metal gate pattern.

**[0070]** Hereinafter, the effect of the exemplary methods for curing or reducing etch damage caused at the edges of the metal gate pattern and reducing or eliminating punch-through defects in the gate insulating layer will be described. FIGS. 12A and 12B are photographs illustrating the thickness of a gate oxide layer formed at edges and the center, respectively, of a gate according to exemplary embodiments of the present invention. That is, a silicon oxide layer is formed as a capping layer to the thickness of 100 Å on the metal gate pattern having the gate length of 90 nm.

**[0071]** As shown in FIG. 12A, the gate oxide layer has the thickness of 91 Å at the edges of the gate pattern, and as shown in FIG. 12B, the gate oxide layer has the thickness of 63 Å at the center of the gate pattern. As compared with FIGS. 11A and 11B, the gate pattern is oxidized to the same extent enough to cure etching damages at the edges of the gate pattern. However, the thickness of the gate oxide layer is increased by only 10 Å or less at the center of the gate pattern, thus illustrating that punch-through of the gate oxide layer may be reduced.

**[0072]** While the invention has been particularly shown and described with reference to exemplary embodiments thereof, it should be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.